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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/611,940	LASSER, MENAHEM	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 21-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,18,22-35,38-41,44,45 and 47-51* is/are rejected.

7)☒ Claim(s) *14-17,36,37,42,43 and 46* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1-18, and 21-51 are pending in the application.

Claims 19-20 are canceled.

Claims 1, 8, 16-18, 24-25, 30, 39, 46-47 are amended.

Claim 51 is new.

Claims 14-17, 36-37, 42-43, and 46 are objected to.

Claims 1-13, 18, 22-35, 38-41, 44-45 and 47-51 are rejected.

Response to Amendment

2. Applicant's arguments filed on 9 November 2005 have been fully considered but they are not persuasive. Therefore, the rejections made in the previous office action are maintained, and restated below, with changes as needed to address the amendments.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 18 and 21-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Suzuki (US Patent 6,601,139 B1).

As for claim 18, Suzuki teaches a computer system comprising:

a processor (Fig. 3, element 11);

a bus (Fig. 3, the bus connects the processor to the removable media device, along with the other components illustrated in the figure) permanently operationally connected to the processor;

at least one memory device including:

a first, directly executable memory for storing boot code of a computer (Fig. 5, ROM area (elements 2a1-2a5). Note in col. 8, lines 17-28 – the boot area is stored directly after the lead-in area, which is stored on the ROM. Referring to figure 4, the ROM area is comprised of the lead-in area and the pre-mastered area. The latter contains the boot area as shown in Fig. 4).

a second memory (Fig. 5, RAM area (element 2b); and

a respective connector for reversible operationally connecting said two memories and said bus to said computer (The removable media device (Fig. 3 element 10) is connected to the system bus via a single interface – col. 7, lines 7-20) in order to exchange signals between the processor and the first and second memories. Also note in col. 7, lines 18-20 – Suzuki discusses his media device as including a PCMIA card. A PCMIA card's interface is inherently reversible.

Conversely, each of the ROM areas as shown in Fig. 5 could be considered separate memories (i.e. ROM area #1 is the first memory, and ROM area #2 is the second memory).

wherein the computer system lacks a Basic Input Output System (BIOS) having a permanent operation connection to said bus (Fig. 3 discloses a basic media access program, however no BIOS is contained within the computer (element 1).

Further, In col. 1, line 66 through col. 2, lines 9 Suzuki defines BIOS as an interface or system that comprises the necessary device drivers for controlling a system (i.e. personal computer). In col. 5, lines 51-65, Suzuki teaches the hardware only including only a basic medium access program (BMAP) in a simple form, and all other software and content as being placed on a removable medium in self-contained form. He continues by teaching the device drivers themselves as being stored on in the ROM area of the removable medium in col. 9, lines 44-47 (i.e. the system must rely on the ROM areas of the disc for the drivers, rather than locating them in the BMAP). Suzuki further discusses the boot area (containing essential elements of the system loader) as being stored on the removable disc (col. 9, lines 29-42). These are just two of many other examples of the distinction drawn between a BIOS and Suzuki's BMAP.

It is worthy to note that Applicant further describes the BIOS as containing boot code, which comprising driver information (see page 2, lines 8-22). The

drivers as taught by Suzuki are stored on the removable media drive (not the BMAP), therefore Suzuki's BMAP and Applicant's BIOS are dissimilar.

As for claim 21, Suzuki discloses the computer system of claim 18, wherein, in each said at least one memory device, said respective second memory is for storing a respective operating system for the computer system (ROM area #2 stores the OS – col. 9. lines 45-48).

As for claim 22, Suzuki discloses the computer system of claim 21, comprising a plurality of said memory devices (Fig. 1, elements 21-24 disclose multiple removable media devices).

As for claim 23, Suzuki discloses the computer system of claim 22, wherein all said respective operating systems are different (col. 10, lines 55-64) – various different OS can be stored on different disks.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6, 39-41, 44, 47, 50-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki in further view of Stewart et al., hereinafter Stewart (US Patent 5,815,706).

As for claim 1 and 51, Suzuki teaches a memory device (and computer system) comprising:

a processor (Fig. 3, element 11);

a bus (Fig. 3, the bus connects the processor to the removable media device, along with the other components illustrated in the figure) permanently operationally connected to the processor;

at least one memory device including:

a first, directly executable memory for storing boot code of a computer (Fig. 5, ROM area (elements 2a1-2a5). Note in col. 8, lines 17-28 – the boot area is stored directly after the lead-in area, which is stored on the ROM. Referring to figure 4, the ROM area is comprised of the lead-in area and the pre-mastered area. The latter contains the boot area as shown in Fig. 4).

a second memory (Fig. 5, RAM area (element 2b); and

a respective connector for reversible operationally connecting said two memories and said bus to said computer (The removable media device (Fig. 3 element 10) is connected to the system bus via a single interface – col. 7, lines 7-20) in order to exchange signals between the processor and the first and second memories. Also note in col. 7, lines 18-20 – Suzuki discusses his media device as including a PCMIA card. A PCMIA card's interface is inherently reversible.

Conversely, each of the ROM areas as shown in Fig. 5 could be considered separate memories (i.e. ROM area #1 is the first memory, and ROM area #2 is the second memory).

Wherein, in each said at least one memory device, said respective first memory is for storing respective boot code for the computer system (Fig. 5, ROM area (elements 2a1-2a5). Note in col. 8, lines 17-28 – the boot area is stored directly after the lead-in area, which is stored on the ROM. Referring to figure 4, the ROM area is comprised of the lead-in area and the pre-mastered area. The latter contains the boot area as shown in Fig. 4).

Suzuki however fails to teach said boot code including code that is executed first by said computer when said computer is powered up.

Stewart however teaches a computer system with plug-in override of system ROM which includes a boot card (inserted into a connector of the computer) used to circumvent the boot memory resident on the motherboard of the computer, hence allowing the user to boot directly from the detachable card (note Stewart defines the rebooting as turning the computer off, then on, just as claimed by Applicant) – col.5 line 65 through col. 6, line 5.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Suzuki to incorporate Stewart's system of boot override in his own information processing apparatus with removable drive(s). With this combination, the apparatus could execute the boot code stored in Suzuki's first memory directly during startup (i.e. the BMAP would be circumvented). With this combination, Suzuki would benefit by exploiting the advantageous new capabilities for update and/or restoration of system software as taught by Stewart (col. 1, lines 43-50). Further, by using the "boot card" approach as taught by Stewart, an end user of Suzuki's apparatus would not

need to take the "hands-on contact" approach of removing the system ROM chip in order to upgrade or repair the system's boot ROM – col. 3, lines 47-52), an approach that not desirable for some users. It is worthy to note that Stewart intended his system to specifically include small portable computers such as Suzuki's apparatus – col. 1, lines 42-50).

As for claim 2, Suzuki teaches the device of claim 1, wherein said operational connection is reversible (col. 7, lines 18-20 – Suzuki discusses a PCMIA card (a PCMIA card interface is inherently reversible)).

As for claim 3, Suzuki teaches the device of claim 1, wherein said operational connection is permanent (col. 7, lines 18-20 – Suzuki discusses a PCMIA card which contains a permanent connection).

As for claim 4, Suzuki teaches the device of claim 1, wherein said first memory is a read-only memory (Fig. 5, elements 2a1-2a5).

As for claim 5, Suzuki teaches the device of claim 1, wherein said second memory is for storing an operating system of said computer (ROM area #2 stores the OS – col. 9. lines 45-48).

As for claim 6, Suzuki teaches the device of claim 1, wherein said second memory is a magnetic disk memory (the removable media can include a magnetic disk – col. 16, lines 15-22).

As for claim 39, Suzuki discloses a method of operating a computer, comprising the steps of:

(a) providing at least one memory device including:

(i) a respective first, directly executable memory (as discussed in the rejection of claim 1 above), and

(ii) a respective second memory (as discussed in the rejection of claim 1);

(b) for each said at least one memory device, storing boot code of the computer in said respective first memory (as discussed in claim 1 above);

(c) operationally connecting one of said at least one memory device to the computer (as discussed in the rejection of claim 1 above); and

(d) executing said boot code that is stored in said respective first memory of said one memory device, by the computer (Fig. 5, ROM area (elements 2a1-2a5). Note in col. 8, lines 17-28 – the boot area is stored directly after the lead-in area, which is stored on the ROM. Referring to figure 4, the ROM area is comprised of the lead-in area and the pre-mastered area. The latter contains the boot area as shown in Fig. 4).

Suzuki however fails to teach said boot code including code that is executed first by said computer when said computer is powered up.

Stewart however teaches a computer system with plug-in override of system ROM which includes a boot card (inserted into a connector of the computer) used to circumvent the boot memory resident on the motherboard of the computer, hence allowing the user to boot directly from the detachable card (note Stewart defines the rebooting as turning the computer off, then on, just as claimed by Applicant) – col.5 line 65 through col. 6, line 5.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Suzuki to incorporate Stewart's system of boot override in his own information processing apparatus with removable drive(s). With this combination, the apparatus could execute the boot code stored in Suzuki's first memory directly during startup (i.e. the BMAP would be circumvented). With this combination, Suzuki would benefit by exploiting the advantageous new capabilities for update and/or restoration of system software as taught by Stewart (col. 1, lines 43-50). Further, by using the "boot card" approach as taught by Stewart, an end user of Suzuki's apparatus would not need to take the "hands-on contact" approach of removing the system ROM chip in order to upgrade or repair the system's boot ROM – col. 3, lines 47-52), an approach that not desirable for some users. It is worthy to note that Stewart intended his system to specifically include small portable computers such as Suzuki's apparatus – col. 1, lines 42-50).

As for claim 40, Suzuki discloses the method of claim 39, wherein said operational connection is reversible (col. 7, lines 18-20 – Suzuki discusses a PCMIA card (a PCMIA card interface is inherently reversible)).

As for claim 41, Suzuki teaches the method of claim 39, further comprising the step of:

for each said at least one memory device, storing an operating system of the computer in said respective second memory (ROM area #2 stores the OS – col. 9. lines 45-48); and

wherein said executing of said boot code includes copying said operating system from said respective second memory of said one memory device to the computer (col. 12, lines 3-7 – The OS is loaded from the disk to the main memory of the computer).

As for claim 44, Suzuki teaches the method of claim 41, wherein a plurality of said memory devices are provided, each said memory device having a respective operating system of the computer stored in said second memory thereof; and wherein all said respective operating systems are different (col. 10, lines 55-64) – various different OS can be stored on different disks.

As for claim 47, Suzuki teaches a method of securing a computer, comprising the steps of:

omitting a Basic Input Output System (BIOS) from the computer (Fig. 3 discloses a basic media access program, however no BIOS is contained within the computer (element 1));

providing a memory device, separate from the computer, said memory device including a first, directly executable memory (as discussed in the rejection of claims 1 and 18 above);

storing boot code of the computer in said first memory (as discussed in the rejection of claims 1 and 18 above); and

reversibly operationally connecting said memory device to the computer (as discussed in the rejection of claims 1 and 18 above).

As for claim 50, Suzuki teaches the method of claim 47, wherein said memory device further includes a second memory;

wherein the method further comprises the step of:

storing an operating system of the computer in said second memory (ROM area #2 stores the OS – col. 9. lines 45-48); and

wherein said executing of said boot code includes copying said operating system from said second memory to the computer (col. 12, lines 3-7 – The OS is loaded from the disk to the main memory of the computer).

4. Claims 7, 45 and 48-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Suzuki and Stewart (as applied to claims 1, 39 and 47 above), and in further view of Solhjell (US Patent 5,542,082).

As for claim 7, though the combined teachings of Suzuki and Stewart meet all of the limitations of claim 1, they fail to specifically teach the second memory as being comprised of a flash memory. Solhjell however discloses a data storage system connected to a host computer capable of storing a boot program, which does include a flash memory (Fig. 3, element 21). It would have been obvious to one of ordinary skill in the art at the time of the invention for Suzuki to have had utilized FLASH memory instead of ROM in the removable media device. Suzuki stores the BIOS in the ROM, therefore he would benefit from Solhjell's system by making it possible to upgrade the BIOS in the field using flash EEPROM as taught by Solhjell in col. 2, lines 33-34.

As for claims 45, 48, and 49 though the combined teachings of Suzuki and Stewart teach all of the limitations of claim 39 and 47, they fails to teach executing said boot code directly from the first memory, by the computer. Solhjell however does teach this limitation in his disclosure (col. 3, lines 65-67 – the boot program may be started in the RAM memory (for the purposes discussed here, the first memory) by the host). It would have been obvious to one of ordinary skill in the art at the time of the invention for Suzuki to further include the option of the host executing the boot code stored in the first memory of Suzuki's system. By doing so, Suzuki would benefit by allowing the storage system to directly update the control program with little or no control from the host system as taught by Sulhjell in col. 3, lines 3-9.

5. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Suzuki and Stewart (as applied to claims 1) and in further view of Ma (US PG Publication 2004/0042735 A1).

As for claim 8, though the combined teachings of Suzuki and Stewart teach all the limitations of claim 1, they fail to include a Universal Serial Bus (USB) controller for supporting communication between the second memory and the computer.

Ma however teaches benefits of implementing a USB connection between two electronic apparatuses (paragraph 0002, lines 1-5). It would have been obvious to one of ordinary skill in the art at the time of the invention for Suzuki to further include a USB controller as a means of interfacing the computer system. By doing so, Suzuki would

benefit by realizing faster communication between the removable media device and the computer system as compared to other standard interface techniques. Ma discusses the benefits of USB in his teachings (in paragraph 004, lines 1-8, Ma discusses the advantages of using USB over other standard techniques with respect to signal transmission speed).

As for claims 9 and 10, though Suzuki discloses storing the read-only driver in the first memory (ROM area #2 stores the device drivers – col. 9, lines 45-47), he does not specifically include USB as the driver type in his teachings. As discussed with respect to the rejection of claim 8 (and the reasons for rejection set forth in that claim), it would have been obvious for Suzuki to further include USB as a type of driver stored in the memory in further view of the teachings of Ma.

6. Claims 24-27, 29 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki (as applied to claim 18 for claim 24), and in further view of Ma.

As for claim 24, though Suzuki teaches all the limitations of claim 18, he fails to include a Universal Serial Bus (USB) controller for supporting communication between the second memory and the computer. Ma however teaches benefits of implementing a USB connection between two electronic apparatuses (paragraph 0002, lines 1-5). It would have been obvious to one of ordinary skill in the art at the time of the invention for Suzuki to further include a USB controller as a means of interfacing the computer system. By doing so, Suzuki would benefit by realizing faster communication between the removable media device and the computer system as compared to other standard

interface techniques. Ma discusses the benefits of USB in his teachings (in paragraph 004, lines 1-8, Ma discusses the advantages of using USB over other standard techniques with respect to signal transmission speed).

As discussed with respect to the rejection of claim 8 (and the reasons for rejection set forth in that claim), it would have been obvious for Suzuki to further include USB as a type of driver stored in the memory in further view of the teachings of Ma.

As for claim 25, though Suzuki discloses a computer peripheral device comprising:

a first component (Fig. 5, ROM elements 2a1-2a5);

a second component separate from said first component (Fig. 5, RAM element 2b). Note that even though the example in Fig. 5 illustrates one disk, Suzuki further teaches the use of separate ROM and RAM ICs to accomplish the same purpose as the disk in Fig. 5. For example, the removable media device as shown in Fig. 5 may be replaced with a hybrid type medium containing separate ROM and RAM ICs (col. 16, lines 15-27). In this embodiment, the media would include two distinct ICs (one ROM, one RAM), which would then be implemented in a similar fashion as discussed previously with the single disk as illustrated in Fig. 5.;

a connector for operationally connecting said first and second components to a computer (the removable media device (Fig. 3 element 10 is connected to the system bus via a single interface – col. 7, lines 7-20));

he fails to include a Universal Serial Bus (USB) controller for supporting communication between the first component and the computer. Ma however teaches benefits of implementing a USB connection between two electronic apparatuses (paragraph 0002, lines 1-5).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Suzuki to further include a USB controller as a means of interfacing the computer system. By doing so, Suzuki would benefit by realizing faster communication between the removable media device and the computer system as compared to other standard interface techniques. The benefits of USB interfaces are taught by Ma and discussed in the rejection of claims 8 and 24 above.

As for claims 26 and 27, Suzuki teaches the first component as being magnetic memory (col. 16, lines 15-22).

As for claims 29 and 31, Suzuki teaches the second component as a directly executable read-only memory for storing boot code (Fig. 5, ROM area (elements 2a1-2a5). Note in col. 9, lines 29-33 – the boot area is stored within the ROM area as shown in Fig. 5. The system loader program within the boot area executes the loading software).

As for claim 32, Suzuki teaches the device of claim 29 wherein operational connection is reversible col. 7, lines 18-20 – Suzuki discusses a PCMIA card (a PCMIA card interface is inherently reversible).

7. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Suzuki and Ma as applied to claim 26 above, in further view of Solhjell.

As for claim 28, though the combined teachings of Suzuki and Ma meet all of the limitations of claim 26, they fail to teach the memory as being comprised of flash memory. Solhjell however discloses a data storage system connected to a host computer capable of storing a boot program, which does include a flash memory (Fig. 3, element 21). It would have been obvious to one of ordinary skill in the art at the time of the invention for Suzuki to have had utilized FLASH memory instead of ROM in the removable media device. Suzuki stores the BIOS in the ROM, therefore he would benefit from Solhjell's system by making it possible to upgrade the BIOS in the field using flash EEPROM as taught by Solhjell in col. 2, lines 33-34.

8. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Suzuki and Stewart as applied to claim 1 above, and in further view of Gene (US Patent 6,757,751 B1).

As for claim 11, though the combined teachings of Suzuki and Stewart meet all of the limitations of claim 1, they fail to teach the removable media device's connector as comprised of a plurality of pins as disclosed by applicant. Gene however, teaches a high-speed, multiple-bank, stacked memory module, which meets all the limitations of claim 11 including:

a first plurality of pins for supporting communication between said first memory and said computer; and a second plurality of pins for supporting communication between said second memory and said computer (Fig. 3, multiple memory modules are illustrated each connected to the CPU, each with unique I/O leads – Col. 7, line 65 through col. 8 line 6).

As for claim 12, Gene discloses the first and second plurality of pins as being separate (Fig. 3, multiple memory modules are illustrated, each connected to the CPU with separate I/O leads – Col. 7, line 65 through col. 8 line 6)

As for claim 13, Gene discloses at least one pin as being shared between each of the memory units (Fig. 3, the clock signal is common to each memory unit, likewise in col.8, lines 1-13 Gene discusses shared control and I/Os between two different banks).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Suzuki to implement Gene's system on the example Suzuki gives in col. 16 lines 15-25 of a removable media device being implemented in the form of a memory card. By doing so, Suzuki would benefit from Gene's system by exploiting the use of shared pins for each of the memory units, which in turn will minimize the number of I/O connections needed for the interface, which in turn will decrease the cost and improve the yield of the memory used for the media card as taught by Gene (col. 2, lines 5-15).

9. Claims 33-35 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Suzuki and Ma as applied to claim 25 above, and in further view of Gene (US Patent 6,757,751 B1).

As for claim 33, though Suzuki and Ma teach all of the limitations of claim 25, they fail to teach the removable media device's connector as comprised of a plurality of pins as disclosed by applicant. Gene however, teaches a high-speed, multiple-bank, stacked memory module, which meets all the limitations of claims 11 and 25 including:

a first plurality of pins for supporting communication between said first memory and said computer; and a second plurality of pins for supporting communication between said second memory and said computer (Fig. 3, multiple memory modules are illustrated each connected to the CPU, each with unique I/O leads – Col. 7, line 65 through col. 8 line 6).

As for claim 34, Gene discloses the first and second plurality of pins as being separate (Fig. 3, multiple memory modules are illustrated, each connected to the CPU with separate I/O leads – Col. 7, line 65 through col. 8 line 6)

As for claim 35, Gene discloses at least one pin as being shared between each of the memory units (Fig. 3, the clock signal is common to each memory unit, likewise in col.8, lines 1-13 Gene discusses shared control and I/Os between two different banks).

As for claim 38, Gene discloses the second plurality of pins as including separate pins for address and data signals (col. 8, lines 5-13).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Suzuki to implement Gene's system on the example Suzuki gives in col. 16 lines 15-25 of a removable media device being implemented in the form of a memory card. By doing so, Suzuki would benefit from Gene's system by exploiting the use of shared pins for each of the memory units, which in turn will minimize the number of I/O connections needed for the interface, which in turn will decrease the cost and improve the yield of the memory used for the media card as taught by Gene (col. 2, lines 5-15).

10. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Suzuki and Ma as applied to claim 29 above, and in further view of Zimmer et al. (hereinafter Zimmer) US PG Publication 2005/0021968 A1.

Though the combined teachings of Suzuki and Ma meet all of the limitations of claim 29, they fail to teach the connector as supporting a Low Pin Count (LPC) protocol for the second component as recited in claim 30. Zimmer however teaches a method for performing a trusted BIOS update with the use of an LPC protocol, which can be launched from a removable media drive (paragraph 0023, lines 1-7). It would have been obvious to one of ordineary skill in the art at the time of the invention for Suzuki to further include Zimmer's method of securing a BIOS update via the LPC protocol. By doing so, Suzuki would benefit from Zimmer's verification and authentication of the boot (or BIOS) information stored on the removable media device, which in turn would prevent the problems associated with receiving un-authentic or corrupt boot images (paragraph 003, lines 5-13).

Response to Arguments

11. Applicant's arguments filed on 9 November 2005 with respect to the rejections under 35 USC 102(e) and 35 USC 103(a) have been fully considered but they are not persuasive.

12. Under the heading "§ 102(e) Rejections – Suzuki '139", Applicant has agreed to amend claims 1, 18 and 39 in further view of the art cited by Examiner. Furthermore, all arguments with respect to the newly amended claims have been addressed above.

As for claim 47, Applicant asserts that the BMAP as taught by Suzuki functions as a BIOS, and is permanently mounted in the computer (element 1). Though Applicant and Examiner agree that the BMAP is connected to the computer, Examiner asserts that Suzuki teaches the distinction between his BMAP, and a standard BIOS as commonly known in the art. In col. 1, line 66 through col. 2, lines 9 Suzuki defines BIOS as an interface or system that comprises the necessary device drivers for controlling a system (i.e. personal computer). In col. 5, lines 51-65, Suzuki teaches the hardware only including only a basic medium access program (BMAP) in a simple form, and all other software and content as being placed on a removable medium in self-contained form. He continues by teaching the device drivers themselves as being stored on in the ROM area of the removable medium in col. 9, lines 44-47 (i.e. the system must rely on the ROM areas of the disc for the drivers, rather than locating them in the BMAP). Suzuki further discusses the boot area (containing essential elements of the system loader) as being stored on the removable disc

(col. 9, lines 29-42). These are just two of many other examples of the distinction drawn between a BIOS and Suzuki's BMAP.

It is worthy to note that Applicant further describes the BIOS as containing boot code, which comprising driver information (see page 2, lines 8-22). The drivers as taught by Suzuki are stored on the removable media drive (not the BMAP), therefore Suzuki's BMAP and Applicant's BIOS are not the same as suggested by Applicant.

Applicant's argument that the claims depending on independent claims 1, 18, 39, and 47 are allowable is rendered moot, as the Examiner has shown each of these independent claims to be rejected.

13. Under the heading "§ 103(a) Rejections – Suzuki '139 in view of Solhjell '082", argument that the claims depending on independent claims 1, 39, and 47 are allowable is rendered moot, as the Examiner has shown each of these independent claims to be rejected.

14. Under the heading "§ 103(a) Rejections – Suzuki '139 in view of Ma '735", argument that the claims depending on independent claims 1 and 18 are allowable is rendered moot, as the Examiner has shown each of these independent claims to be rejected.

As for claim 25, Applicant asserts that the obvious way to connect a computer peripheral with two separate components to a computer via a USB connection is to provide either a common USB controller for both components or two separate USB controllers for the two components so that both components

can have USB connection to the computer. Applicant further asserts that claim 25 is patentably distinct over the cited prior art of record (herein Suzuki in further view of Ma), because the claim recites that the computer peripheral includes only one USB controller and that that USB controller supports communication only between the first component and the computer, and not between the second component and the computer.

The Examiner maintains the assertion that it would have been obvious for Suzuki to include Ma's USB connection to connect only the first of the two distinct components (ROM IC and RAM IC as discussed in Suzuki col. 16, lines 7-17) to his computer system. Referring again to his teachings, Ma asserts that USB can be used to connect two electronic apparatuses (i.e. a computer and a computer peripheral apparatus) – Also note all USB connections must be inherently controlled by a controller, otherwise they would fail to function. This teaching would allow for one of the ICs (either ROM or RAM) to be connected to Suzuki's system via a USB connection. Ma further teaches the need for a hub to connect more than one component (i.e. both of Suzuki's ICs) to the computer. Examiner's original assertion did not indicate that it would have been obvious for Suzuki to use the hub in conjunction with a USB connection as taught Ma to provided communication between both components to the computer, but rather use Ma's system of communicating between one (emphasis added) component and the computer via his teaching to allow for the communication between one and only one device via USB.

15. Arguments made under the three remaining "§ 103(a) Rejections ..." headings are rendered moot, as the Examiner has shown each of the independent claims to be rejected.

16. With respect to arguments made under the heading "Objections", Examiner removes all of the objections previously set forth in view of applicant's amendments/remarks.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Fulghum teaches a system for upgrading functionality of a peripheral device utilizing a removable ROM having relocatable object code.

18. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER